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Notice of Allowability	Application No. 10/729,227	Applicant(s) KIM, IN-SU	
	Examiner Toniae M. Thomas	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 07 March 2005*.

2. ☒ The allowed claim(s) is/are *1 and 3-6*.

3. ☒ The drawings filed on *05 December 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Mary Wilczewski
Primary Examiner

Reasons for Allowance

Claim 1 has been amended to recite,

> A method of manufacturing a semiconductor device comprising: forming a multi-layered insulating structure on a semiconductor substrate, the multi-layered insulating structure including an upper oxide layer, an intermediate nitride layer and a lower oxide layer; forming an opening in the insulating structure to expose a field region of the semiconductor substrate; forming a trench in the field region of the semiconductor substrate; forming a groove on an edge portion of the intermediate nitride layer of the multi-layered insulating structure; depositing a liner insulating layer in a desired thickness on surfaces of the trench, on an edge of the lower oxide layer, in the groove of the edge portion of the intermediate nitride layer, and on an edge of the upper oxide layer; and filling the groove and the trench with an oxide layer.

The prior art of record does not anticipate or render obvious a method of manufacturing a semiconductor device substantially as recited in claim 1. As evidenced by the prior art, it is known to: form a multi-layered insulating structure on a semiconductor substrate, the multi-layered insulating structure including an upper oxide layer, an intermediate nitride layer, and a lower oxide layer; form a trench in an exposed field region of the substrate through the multi-layered structure; and form a groove on an edge portion of the intermediate nitride layer of the multi-layered structure (e.g. see prior art reference US 6,153,479, Liao et al. - figs. 2A-2E and accompanying text).[1] However, the prior art of record fails to anticipate, teach or suggest - either separately or combined - a method comprising the combination of steps substantially as claimed, the combination of steps including *depositing a liner insulating layer on surfaces of the trench, on an edge of the lower oxide layer, in*

[1] The Liao et al. patent was made of record in the Office action mailed on 18 November 2004.

the groove of the edge portion of the intermediate nitride layer, and on an edge of the upper oxide layer, as recited in claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
15 May 2005

Mary Wilczewski
Primary Examiner